

Claim 1.

A semiconductor integrated circuit device, comprising:  
impurity diffusion regions formed as source and drain on a  
semiconductor substrate;

5 a first conductive layer having a first resistivity formed on said impurity  
diffusion regions;

a first contact hole group connecting said first conductive layer and said  
impurity diffusion region;

a second conductive layer having a second resistivity formed on said first  
10 conductive layer; and

a second contact hole group connecting said first conductive layer and  
said second conductive layer at an upper part of said impurity diffusion region,  
wherein

a total number of contact holes is respectively different between said first  
15 contact hole group and said second contact hole group.

Claim 2.

The semiconductor integrated circuit device as disclosed in claim 1,  
wherein said first resistivity is higher than said second resistivity, and a total  
20 number of holes in said first contact hole group is more than a total number of  
holes in said second contact hole group.

Claim 3.

A semiconductor integrated circuit device, comprising:

25 a source region formed on a semiconductor substrate;

a first conductive layer having a first resistivity formed on said source  
region;

a first contact hole group connecting said source region and said first  
conductive layer;

30 a second conductive layer having a second resistivity formed on said first  
conductive layer;

a second contact hole group, on an upper part of said source region,  
connecting said first conductive layer and said second conductive layer;

a drain region formed on a semiconductor substrate;  
a third conductive layer having said first resistivity formed on said drain region;

a third contact hole group connecting said drain region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third conductive layer;

a fourth contact hole group, on an upper part of said drain region, connecting said third conductive layer and said fourth conductive layer;

10 wherein

a total number of contact holes is respectively different between said first contact hole group and said third contact hole group, and

a total number of contact holes is respectively different between said second contact hole group and said fourth contact hole group.

15 Claim 4.

The semiconductor integrated circuit device as disclosed in claim 3, wherein the total number of contact holes in said first contact hole group is the same as the total number of contact holes in said third contact hole group, and  
20 the total number of contact holes in said second contact hole group is the same as the total number of contact holes in said fourth contact hole group.

Claim 5.

The semiconductor integrated circuit device as disclosed in claim 4,  
25 wherein said first resistivity is higher than said second resistivity, the total number of contact holes for said first contact hole group and said third contact hole group is more than the total number of contact holes for said second contact hole group and said fourth contact hole group.

30 Claim 6.

A semiconductor integrated circuit device, comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing

side by side in a second direction;

a first conductive layer having a first resistivity formed on said first impurity diffusion region;

a first contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said first impurity diffusion region and said first conductive layer;

a second conductive layer having a second resistivity formed on said first conductive layer;

a second contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said first conductive layer and said second conductive layer, at an upper part of said first impurity diffusion region;

a third conductive layer having said first resistivity formed on said second impurity diffusion region;

a third contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said second impurity diffusion region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third first conductive layer; and

a fourth contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said third conductive layer and said fourth conductive layer, at an upper part of said second impurity diffusion region, wherein

said first contact hole group is arranged between neighboring contact holes of said second contact hole group, and

said third contact hole group is arranged between neighboring contact holes of said fourth contact hole group.

#### Claim 7.

The semiconductor integrated circuit device as disclosed in claim 6, wherein

a distance between a contact hole of said first contact group and a contact hole of said second contact hole group adjacent to the contact hole of said first

contact hole group is <sup>FIXED</sup> ed value, and

a distance between a contact hole of said third contact group and a contact hole of said fourth contact hole group adjacent to the contact hole of said third contact hole group is a fixed value.

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Claim 8.

The semiconductor integrated circuit device as disclosed in claim 6, wherein

an interval between contact holes of said first contact group situated  
10 between neighboring holes of said second contact hole group is a fixed value, and

an interval between contact holes of said third contact group situated  
between neighboring holes of said fourth contact hole group is a fixed value.

15 Claim 9.

The semiconductor integrated circuit device as disclosed in claim 6, wherein said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second  
20 impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said  
first contact hole group extremely close to said first side,

a second distance defined as a distance from said second side to an edge  
of said first contact hole group extremely close to said second side, and

25 a third distance defined as a distance from said third side to an edge of  
said first contact hole group extremely close to said third side

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first  
30 impurity diffusion region,

a fourth distance defined as a distance from said fourth side to an edge of  
said third contact hole group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of

said third contact hole ~~up~~ extremely close to said fifth ~~side~~ and

a sixth distance defined as a distance from said sixth side to an edge of said third contact hole group extremely close to said sixth side, wherein

said first distance and said second distance are both larger than said third distance, and

said fourth distance and said fifth distance are both larger than said sixth distance.

#### Claim 10.

10 The semiconductor integrated circuit device as disclosed in claim 6, wherein

said first contact hole group is divided into a plurality of subgroups according to a predetermined fixed number of contact holes, and each subgroup is arranged between adjacent contact holes of said second contact hole group, 15 and

said third contact hole groups are divided into a plurality of subgroups according to a predetermined fixed number of contact holes, and each subgroup is arranged between adjacent contact holes of said fourth contact hole group.

#### 20 Claim 11.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

a distance from contact holes of said first contact hole group and contact holes of said second contact hole group adjacent to holes of said first contact 25 hole group, has a fixed value and

a distance from contact holes of said third contact hole group and contact holes of said fourth contact hole group adjacent to holes of said third contact hole group, has a fixed value.

#### 30 Claim 12.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

an interval between contact holes of said first contact hole groups

adjacent contact  
contact  
arranged between adjacent contact holes of said second contact hole group has a fixed value, and

an interval between contact holes of said third contact hole groups arranged between adjacent contact holes of said fourth contact hole group has a fixed value.

Claim 13.

The semiconductor integrated circuit device as disclosed in claim 10, wherein

10 said first impurity diffusion region has  
a first side and a second side running in said second direction,  
a third side running in said first direction and opposite to said second  
impurity diffusion region,  
a first distance defined as a distance from said first side to an edge of said  
15 first contact hole group extremely close to said first side,  
a second distance defined as a distance from said second side to an edge  
of said first contact hole group extremely close to said second side, and  
a third distance defined as a distance from said third side to an edge of  
said first contact hole group extremely close to said third side  
20 said second impurity diffusion region has  
a fourth side and a fifth side running in said second direction,  
a sixth side running in said first direction and opposite to said first  
impurity diffusion region,  
a fourth distance defined as a distance from said fourth side to an edge of  
25 said third contact hole group extremely close to said fourth side,  
a fifth distance defined as a distance from said fifth side to an edge of  
said third contact hole group extremely close to said fifth side, and  
a sixth distance defined as a distance from said sixth side to an edge of  
said third contact hole group extremely close to said sixth side, wherein  
30 said first distance and said second distance are both larger than said third  
distance, and  
said fourth distance and said fifth distance are both larger than said sixth

distance.

Claim 14.

5 A semiconductor integrated circuit, comprising a first transistor for input and a second transistor for output, said first transistor and said second transistor being connected to an input/output terminal, said first transistor comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing  
10 side by side in a second direction;

a first conductive layer having a first resistivity formed on said first impurity diffusion region;

a first contact hole group having a plurality of contact holes arranged side by side in said first direction, for connecting said first impurity diffusion region  
15 and said first conductive layer;

a second conductive layer having a second resistivity formed on said first conductive layer;

a second contact hole group, having a plurality of contact holes arranged side by side in said first direction for connecting said first conductive layer and  
20 said second conductive layer, at an upper part of said first impurity diffusion region;

a third conductive layer having said first resistivity formed on said second impurity diffusion region;

a third contact hole group having a plurality of contact holes arranged  
25 side by side in said first direction, for connecting said second impurity diffusion region and said third conductive layer;

a fourth conductive layer having said second resistivity formed on said third first conductive layer; and

a fourth contact hole group, having a plurality of contact holes arranged  
30 side by side in said first direction for connecting said third conductive layer and said fourth conductive layer, at an upper part of said second impurity diffusion region, wherein

said first contact hole group has a predetermined fixed number of contact

holes arranged between each neighboring contact hole of said second contact hole group, and has a first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and

said third contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said fourth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and said second transistor comprising:

a third impurity diffusion region and a fourth impurity diffusion region formed on a semiconductor substrate, extending in a third direction and standing side by side in a fourth direction;

a fifth conductive layer having a first resistivity formed on said third impurity diffusion region;

a fifth contact hole group having a plurality of contact holes arranged side by side in said third direction, for connecting said third impurity diffusion region and said fifth conductive layer;

a sixth conductive layer having a second resistivity formed on said fifth conductive layer;

a sixth contact hole group, having a plurality of contact holes arranged side by side in said third direction for connecting said fifth conductive layer and said sixth conductive layer, at an upper part of said third impurity diffusion region;

a seventh conductive layer having said first resistivity formed on said fourth impurity diffusion region;

a seventh contact hole group having a plurality of contact holes arranged side by side in said third direction, for connecting said fourth impurity diffusion region and said seventh conductive layer;

an eighth conductive layer having said second resistivity formed on said seventh first conductive layer; and

an eighth contact hole group, having a plurality of contact holes arranged side by side in said third direction for connecting said seventh conductive layer and said eighth conductive layer, at an upper part of said fourth impurity diffusion region, wherein

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said fifth contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said sixth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes, and

5 said seventh contact hole group has a predetermined fixed number of contact holes arranged between each neighboring contact hole of said eighth contact hole group, and has said first fixed interval between said predetermined number of arranged contact holes and adjacent contact holes.

10 Claim 15.

The semiconductor integrated circuit as disclosed in claim 14, having a first side, for said first impurity diffusion region, running in said first direction and opposite to said second impurity diffusion region;

15 a second side, for said second impurity diffusion region, running in said first direction and opposite to said first impurity diffusion region;

a third side, for said third impurity diffusion region, running in said third direction and opposite to said fourth impurity diffusion region;

a fourth side, for said fourth impurity diffusion region, running in said third direction and opposite to said third impurity diffusion region;

20 a first distance defined as a distance between said first side and said second side; and

a second distance defined as a distance between said third side and said fourth side, wherein

said first distance and said second distance are equal.

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